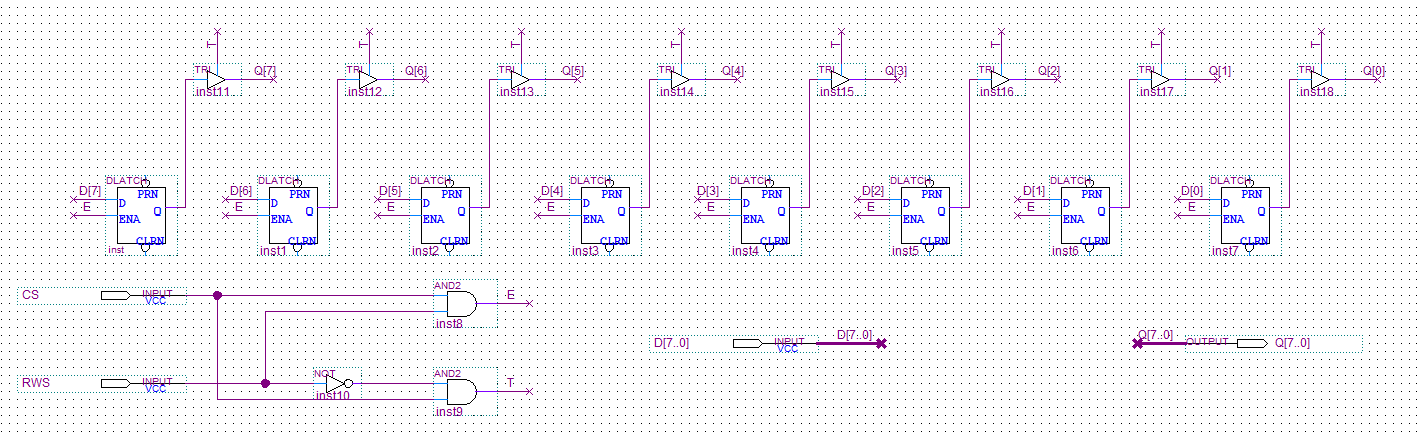
**THIẾT KẾ RAM32X8**

\*Thiết kế Cell Ram 8bit sử dụng D-Latch

-Schematic:



-Đóng gói:

Diagram

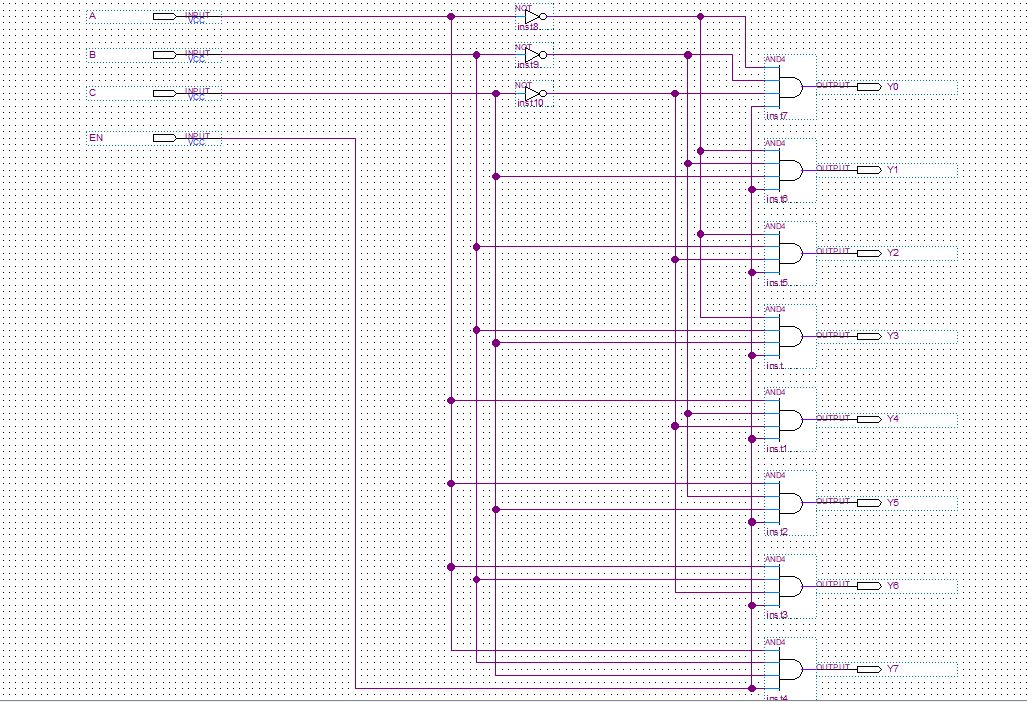
Description automatically generated

\*Decoder 3-to-8

-Truth table:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

-Schematic:



-Đóng gói:

Diagram, schematic

Description automatically generated

\*Decoder 2-to-4:

-Truth table:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

-Schematic:

Calendar

Description automatically generated

-Đóng gói:

Diagram

Description automatically generated

\*Thiết kế Ram 8x8 sử dụng 8 cell ram và Decoder 3-to-8:

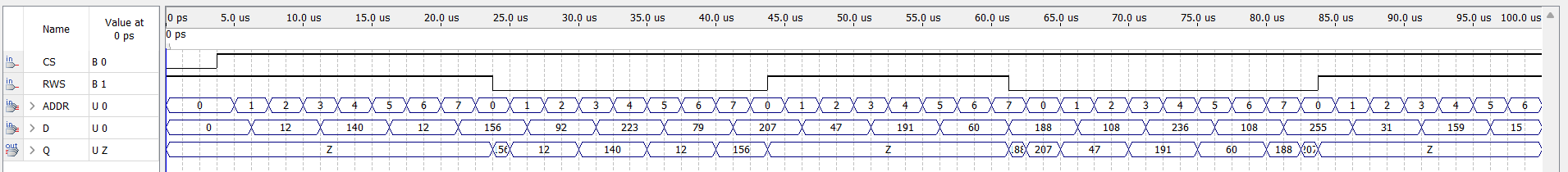
A picture containing diagram

Description automatically generated-Schematic:

-Đóng gói:

A picture containing diagram

Description automatically generated

-Kết quả mô phỏng:

\*Thiết kế Ram 32x8 sử dụng Ram 8x8 và Decoder 2-to-4:

-Schematic:

Diagram

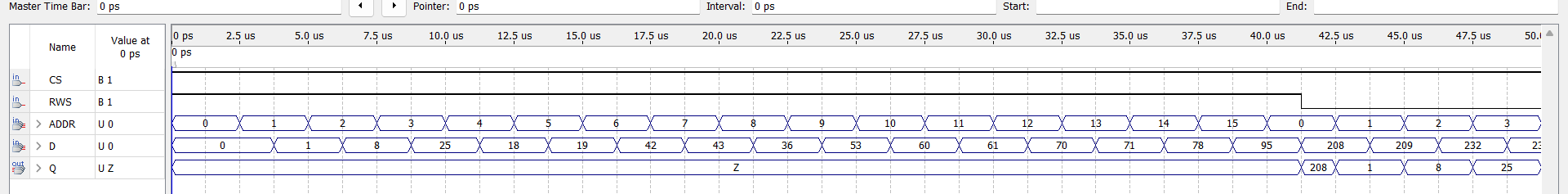
Description automatically generated

-Đóng gói:

Calendar

Description automatically generated with medium confidence

-Kết quả mô phỏng:



Chart, scatter chart

Description automatically generated

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